REMARKS

By this response claims 33, 35, 37, 42, and 44 have been amended. Claims 33-46 remain pending. Reconsideration of the application as amended is respectfully requested.

Objections to the Claims

Claims 33, 35, and 37 have been objected to as containing informal language. Claim 44 has been objected to as containing a numbering error.

The amendments to claims 33, 35, 37, and 44 overcome the Examiner's objections.

Rejections under 35 USC §102(b)

Claims 33-35, 37-40, and 42-45 have been rejected under 35 USC §102(b) as being anticipated by JP 6-232537. JP 6-232537 discloses a method which allows accurate trimming of a resistor independent of the circuit to which the resistor is attached. If the resistor is not separated from the circuit and from other resistors in the circuit, it can be trimmed but the trimming is not as exact (translation, ¶[0001] - [0004]). JP 6-232537 concerns a particular method for connecting the circuit after trimming the resistor comprising the use of solder paste rather than using a soldering iron, which is excessively large for fine-pitch devices (¶[0007] - [0008])).

The present invention as claimed comprises novel and nonobvious differences over the invention of JP 6-232537. Claim 33 recites "...with the first and second circuits electrically separate from each other, performing an electrical operation on the first circuit with a voltage sufficient to damage the second circuit when applied to the first circuit with the first and second circuits electrically connected to each other...".

The translation of JP 6-232537 does not indicate how the resistor is trimmed, but does not teach that a voltage is applied to the resistor in order to trim the resistor. Thus the recitation from claim 33 of "with the first and second circuits electrically separate from each other, performing an electrical operation on the first circuit *with a voltage*" is not met, and claim 33 and rejected claims 34 and 35 which depend therefrom are allowable under 35 USC §102(b) for this reason alone.

Further, JP 6-232537 indicates that trimming is possible with the circuits connected (¶ 3), albeit with decreased precision. Thus even if a voltage is used to trim the resistor, the recitation of performing the operation on the first circuit "with a voltage sufficient to damage the second circuit when applied to the first circuit with the first and second circuits electrically connected to each other" is not met.

JP 6-232537 does not recite that the method of trimming the resistor is different if the two circuits are attached, just that it is more accurate with them separate. Because JP 6-232537 indicates the resistor can be trimmed with the resistor attached to the circuit, it must be assumed that the trimming the resistor with the circuits attached does not damage the circuit, otherwise it would not be done. Thus claim 33, and claims 34 and 35 which depend therefrom, are further allowable over JP 6-232537.

With regard to claim 34, the Examiner indicates that JP 6-232537 discloses the use of a ball bond. However, JP 6-232537 consistently recites the use of a solder paste applied to the electrodes which is then heated and fused (¶ [0009], page 2 of the translation, for example). It is submitted that this is clearly different from the use of a ball bond, which is not a solder paste which is applied and then heated to fuse the paste. Thus claim 34 is further allowable over JP 6-232537 under 35 USC §102(b).

Claims 37-40 have been rejected under 35 USC §102(b) over JP 6-232537. The Examiner states that the translation of JP 6-232537 teaches the features described in claim 37, for example "primary and redundant memory cell locations," "antifuse circuitry," "a first conductor electrically connected with the antifuse circuitry," "applying a sufficient voltage to the antifuse circuitry to program the antifuse circuitry," etc. It is not evident from the translation supplied by the Examiner that JP 6-232537 comprises any of these features. Another translation is attached hereto as "Exhibit I," which also appears to omit the features described above. This reference appears to discuss the trimming of a resistor on a "hybrid IC" and fails to teach or suggest a redundant memory cell or even a memory device, let alone most of the recitations of rejected claims 37-40. Thus the Examiner's use of JP 6-232537 to reject the present invention as recited in claims 37-40 is respectfully traversed as failing "teach every aspect of the claimed invention either explicitly or impliedly" (MPEP §706.02(IV)) as required for rejection under 35 USC §102(b).

Claim 37 recites "forming a plurality of primary and redundant memory cell locations; forming antifuse circuitry which allows selection of the redundant memory cell locations; forming voltage sensitive circuitry...; forming a first conductor electrically connected with the antifuse circuitry; forming a second conductor electrically connected with the voltage sensitive circuitry...; while the first and second conductors are electrically separated, applying a voltage to the antifuse circuitry to program the antifuse circuitry, wherein the voltage is sufficient to damage the voltage sensitive circuitry when applied to the antifuse circuitry when the first and second conductors are electrically connected...". Because JP 6-232537 fails to teach, suggest, or even imply various claimed features such as "a redundant memory cell location," "antifuse circuitry," "a first conductor electrically connected with the antifuse circuitry," claim 37 and rejected claims 38-40 which depend therefrom are allowable over JP 6-232537 for this reason alone.

As discussed relative to the rejections of claims 33-35 over JP 6-232537 under 35 USC §102(b), JP 6-232537 fails to teach or suggest the similar recitation "...while the first and second conductors are electrically separated, applying a voltage to the antifuse circuitry to program the antifuse circuitry, wherein the voltage is sufficient to damage the voltage sensitive circuitry when applied to the antifuse circuitry when the first and second conductor are electrically connected." JP 6-232537 indicates less precise trimming of the resistor is possible when the circuits are connected. As claim 37 recites that such use "is sufficient to damage the voltage sensitive circuitry," and the resistor trimming of the reference is not sufficient to damage the circuitry, claim 37 and claims 38-40 which depend therefrom are further allowable over JP 6-232537 under 35 USC §102(b).

Similar to claim 34, claim 37 recites the use of a ball bond. Because solder paste and a ball bond are not the same as discussed relative to the rejection above of claim 34, claim 37 is further allowable over JP 6-232537 under 35 USC §102(b).

Claims 42-45 have been rejected over JP 6-232537 under 35 USC §102(b). Claim 42 recites a method comprising "...fabricating the common conductor with a physical opening to provide an open circuit between the first and second circuits, such that the first circuit is sufficiently isolated from the second circuit to provide protection for the first circuit from a voltage applied to the second circuit which is sufficient to damage the first circuit when applied to the second circuit with the physical opening bridged...". JP 6-232537 does not discuss the application of a voltage to trim the resistor, and thus claim 42 and claims 43-45 which depend therefrom are allowable over JP 6-232537 under 35 USC §102(b).

Further, the resistor may be less accurately trimmed with the circuits connected, and thus the trimming of the resistor with the circuits attached does not damage the circuit. Thus even if the resistor is trimmed through the application of a voltage to the resistor, any voltage applied is not "sufficient to damage the first circuit when applied to the second circuit with the physical opening bridged." Thus the recitations of claim 42 is not met, and claims 42-45 are further allowable over JP 6-232537 under 35 USC §102(b).

Similar to claim 34, claim 44 recites the use of a ball bond. Because solder paste and a ball bond are not the same as discussed relative to the rejection above of claim 34, claim 44 is further allowable over JP 6-232537 under 35 USC §102(b).

Any claims not individually addressed are allowable at least because they depend from an allowable base claim. Thus it is submitted that all of claims 33-35, 37-40, and 42-45 are allowable over JP 6-232537 under 35 USC §102(b).

Rejections under 35 USC §103(a)

Claims 36, 41, and 46 have been rejected under 35 USC §103(a) as being unpatentable over JP 6-232537 in view of applicant's admitted prior art. The use of a lead frame in semiconductor manufacturing is well established.

The cited references fail to teach or suggest many of the features of the claimed invention. Claim 33 from which rejected claim 36 depends recites "...with the first and second circuits electrically separate from each other, performing an electrical operation on the first circuit with a voltage sufficient to damage the second circuit when applied to the first circuit with the first and second circuits electrically connected to each other...". Similar recitations are found in claims 37 and 42 from which rejected claims 41 and 46 depend.

The references in combination fail to teach or suggest the application of a voltage to trim the resistor, thus the claims are allowable over the cited references. Assuming *arguendo* JP 6-232537 uses a voltage to trim the resistance, the references still fail to teach or suggest that the voltage applied is sufficient to damage the circuit. JP 6-232537 discusses trimming the resistor with the two circuit portions connected, but advantageously separates the circuit portions to *more accurately* trim the resistor (page 1, ¶[0003]). Thus the trimming can be accomplished without separating the circuit portions and damage will not occur. Because JP 6-232537 and AAPA in combination fail to teach or suggest all of the features taught by the combination of references as required (MPEP §706.02(j)), rejected claims 36, 41, and 46 are allowable under 35 USC §103(a).

As further discussed relative to the rejection under 35 USC §102(b), the combination of references fail to teach or suggest many of the recited elements from the claim 37 from which rejected claim 41 depends, such as "forming a plurality of primary and redundant memory cell locations," "forming antifuse circuitry," and "forming a conductor electrically connected with the antifuse circuitry." Thus claim 41 is further allowable over the combination of references under 35 USC §103(a).

Thus rejected claims 36, 41, and 46 are allowable over JP 6-232537 and AAPA in combination under 35 USC §103(a).

EXHIBIT I

[Translation]

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(54) **Name of Invention:** Method of Short-circuiting Electrode for Closed-circuit Formation

(57) **Summary**

Purpose: To reliably make short circuits in a method for short-circuiting electrodes used in forming paired closed circuits.

Makeup: In forming paired electrodes for making closed circuits in such form that the side where they are connected to the wiring pattern will be narrower than the wiring pattern, from atop these paired electrodes one imprints soldering paste in a region having an area greater than these electrodes, then heats this soldering paste and fuses it so that the above-noted paired electrodes are short-circuited by the fused solder.

Scope of Patent Application

Application Item 1 A method for short-circuiting electrodes used to form closed circuits that is characterized by forming, on a substrate, paired electrodes for forming closed circuits so shaped that their side connected to the wiring pattern is narrower and they face each other across a prescribed gap; they are imprinted from atop the paired electrodes with solder paste in an region with an area larger than those electrodes; and by heating and fusing that solder paste the above-noted paired electrodes for forming closed circuits are short-circuited by the solder.

Detailed Explanation of Invention

0001 Field for Commercial Application This patent relates to a method for short-circuiting electrodes for forming the closed circuits used in the composite-circuit parts of hybrid ICs, etc.

0002 Usual Technology In composite circuit parts such as hybrid ICs, when—for instance—trying to trim resistors connected within closed circuits, one needs to be able to measure the resistance of a single resistor.

0003 However, when other resistors are connected in the closed circuit, the resistance of such a resistor will be affected and one cannot measure the resistance of the very resistor one is trying to trim, so that precise trimming is not possible.

0004 Due to that, one starts out with the resistor one seeks to trim cut off in the part of the wiring pattern forming the closed circuit so that it will not be affected by other resistors, and after that one connects the isolated part of the wiring pattern to form the closed circuit.

0005 Such means of forming closed circuits is a method long followed and is shown in Figure 3. I.e., as shown in Fig. 3(a), one forms paired rectangular electrodes 12,12 for a closed circuit connected to wiring patterns 11,11 on a substrate where a composite circuit part is to be formed. As that does not yet form a closed circuit, it is in a state where, for instance, trimming resistors is possible. Then, when the trimming is done, as shown in Fig. 3(b), one imprints soldering paste 13 from above with an area that encompasses paired electrodes 12. If one then heats and fuses soldering paste 13, electrodes 12, 12 for forming a closed circuit will be short-circuited by fused solder 14, as shown in Fig. 3(c), and the closed circuit will be formed.

0006 Issue the Invention Seeks to Resolve On the other hand, with the recent refining in the lead pitch of the electronic parts mounted on the substrates of integrated circuits, etc., soldering paste has been developed and put to use for such fine pitches to make short circuits unlikely between leads.

0007 And yet, because short circuits are unlikely with such soldering paste due to their nature even between the above-noted electrodes 12,12 for forming closed circuits, forming reliable closed circuits becomes difficult, giving rise to the problem that one must make corrections with each soldering.

0008 Hence, even when using the above-noted kind of soldering paste for fine pitch situations, with this invention the goal is to provide an electrode short-circuiting method for forming closed circuits such that the short-circuiting of these electrodes can be done reliably.

0009 Means to Resolve the Issue To attain such a goal, this invention's short-circuiting method for electrodes used for forming paired electrodes for making closed circuits is distinguished by making such electrodes in such form that the side where they are connected to the wiring pattern is narrower than the wiring pattern and from atop these paired electrodes one imprints soldering paste in a region with an area greater than these electrodes, then heats and fuses this soldering paste so that the above-noted paired electrodes are short-circuited by the fused solder.

0010 Effects By forming the paired electrodes for use in closed circuits in a shape where they are narrower on the wiring pattern side, face each other across a prescribed gap, and by imprinting soldering paste on a region with an area larger than those electrodes and then fusing that paste on the region's outer side where electrodes are narrower than the wiring pattern, drawing it toward the electrodes for closed circuits, it adheres uniformly to the electrode surfaces. So, the amount of fused solder near the electrode gap becomes greater, and one can easily get the paired electrodes short-circuited.

0011 Application example Below, we will explain an example of applying this invention, referring to the figures.

0012 First, as shown in Fig. 1(a), when forming the wiring pattern on a substrate, one simultaneously makes paired electrodes 2,2 for forming a closed-circuit, shaping them so that they are narrower at the side of wiring pattern 1,1 which is connected to that wiring pattern. This pair of electrodes are made facing each other across a gap for instance in the range of 100μm.

0013 Then, after completing such designated processing as trimming of resistors, one imprints from above solder paste 3, as shown in Fig. 1(b), for a fine pitch on a region with an area greater than paired electrodes 2,2 for a closed circuit.

0014 After that, one heats and fuses solder paste 3 so that it covers electrodes 2,2 and the region on the outer side of the narrow part of wiring pattern 1,1 for these electrodes so that it spreads out uniformly; and , as shown

in Fig. 1(c), paired electrodes 2,2 will be shorted by the fused solder 4. Of course, this fused solder gradually cools and hardens.

0015 The shape of electrodes 2,2 for forming closed circuits may also be as shown in Figure 2 as long as their wiring-pattern side 1,1 is narrower. And, needless to say, by forming electrodes 2,2 as explained above there would be cases in which one uses the usual soldering paste as the short-circuiting will be done reliably.

0016 Effectiveness of Invention As will be clear from the above explanation, from having imprinted soldering paste from above over the electrodes as described with this invention, short-circuiting of the paired electrodes for making closed circuits will be done reliably.

Simple Explanation of Figures

Figure 1 is a figure to explain this invention's method of short-circuiting electrodes for making closed circuits. Fig. 1(a) is a plane diagram of the electrodes; Fig. 1(b) illustrates the condition when the soldering paste is imprinted from above the electrodes shown in Fig. 1(a); and Fig. 1(c) shows the conditions after the soldering paste shown in Fig. 1(b) has fused.

Figure 2 is a figure showing another shape of the electrodes used in this invention.

Figure 3 is a figure for illustrating the usual way of short-circuiting such electrodes. Fig. 3(a) is a plane figure of the electrodes for making closed circuits; Fig. 3(b) is a figure showing the condition when the soldering paste has been imprinted from above on the electrodes shown in Fig. 3(a); and Fig. 3(c) shows the conditions after the soldering paste has been fused.

Explanation of Symbols

1, 11 Wiring pattern
2, 12 Electrodes for forming closed circuits
3 Soldering paste
4 Fused solder.